REMARKS

This amendment responds to the office action mailed June 27, 2006. In the office action the Examiner:

- rejected claims 1-2, 6-10, 13-22, 24, 26-27 and 30-32 under 35 U.S.C. 102(b) as anticipated by Olarig et al. (US 6,260,127);
- rejected claims 3 and 23 under 35 U.S.C. 103(a) as being unpatentable over Olarig et al. as applied to claims 1-2 and 22 above, further in view of Sinclair (US 6,578,127);
- rejected claims 4-5 and 25 under 35 U.S.C. 103(a) as being unpatentable over Olarig et al. as applied to claims 1-3 and 22 above, further in view of Sinclair (US 6,578,127); and
- rejected claims 11-12 and 28-29 under 35 U.S.C. 103(a) as being unpatentable over Olarig et al. as applied to claims 1 and 22 above, further in view of Coldewey (US 2004/0133747).

The specification has been amended to correct a typographical error. Claim 2 has been cancelled. Claim 1 has been amended to include the limitations of claim 2. Claim 1 has been further amended to recite that the first memory devices comprise volatile memory devices and the second characteristic includes a usage characteristic selected from the group consisting of a read-mostly characteristic and read-only characteristic. Support for these limitations can be found in the specification for example, at paragraph 0007 and claim 24. Claim 3 has been amended to recite the appropriate dependency. Claim 14 has been amended to correct a typographical error. Claim 23 has been amended to recited that the first memory devices are volatile memory devices and the second memory devices are non-volatile memory devices. Claim 31 has been amended to include the limitations of claim 2 and to recite that the first memory devices comprise volatile memory devices and the second characteristic includes a usage characteristic selected from the group consisting of a read-mostly characteristic and read-only characteristic. Support for these limitations can be found in the specification for example, at paragraph 0007 and claim 24. After entry of this amendment, the pending claims are: claims 1 and 3-32.

Olarig is directed to a method and apparatus for supporting heterogeneous memory in computers. In particular, Olarig is concerned with allowing for the gradual upgrading of SIMMs and DIMMs. See, e.g., column 6, lines 49-57. Olarig contemplates that the different

types of memory modules controlled by his invention are "multiple physical modules" such as DIMMs, SIMMs, EDO DRAMs and the like. See, e.g. column 10, lines 8-28. Olarig does not have first and second interfaces between each of first and second memory devices. Instead, the single interface between the memory modules and memory controller of Olarig is the "memory personality module 300 or RAM personality module." See column 6, line 58 – column 7, 8. Contrary to the requirements of claim 1, Olarig does not disclose a second memory interface adapted to be coupled to non-volatile memory devices. In rejecting previous claim 2, the Examiner cited column 5, lines 19-28 of Olarig. This portion of Olarig discloses that a typical computer system may have an allocation map within non-volatile memory to allow the microprocessor to communicate with other devices. This does not show a second memory interface to be coupled to non-volatile storage. Applicant's review of Olarig also did not find a second memory interface adapted to be coupled to non-volatile memory devices.

Olarig does not disclose directing memory transactions to either a first or second memory interface depending on the characteristics of the transaction, in particular Olarig does not disclose directing memory transactions to one type of memory or another based on the characteristics of the memory transactions. The Office Action cites column 12, lines 30-38 of Olarig for the proposition that Olarig discloses interface logic for directing memory transactions to either the first or second memory interface depending on the characteristics of the transaction, as claimed. This portion of Olarig discloses control logic for a multiplexer or selector. This logic allows Olarig "to detect the type of each physical memory module." Column 11, lines 31-32. The control logic and controller 730 of this portion of Olarig merely cycles through the DIMMs and passes values indicating their presence and type back, eventually to be read by RAM personality module 300. The cited control logic and controller 730 does not direct memory transactions; it merely detects status look-ups; and certainly does not direct memory transactions based on usage characteristics of memory transactions. Applicant's review of Olarig also did not find teachings to direct memory transactions to either a first or second memory interface depending on usage characteristics of the transaction.

It may be helpful to consider the problem that Olarig addresses. In particular, Olarig addresses the situation in which a computer has two similar memory modules (e.g., two DIMMs) that have similar but distinct operating characteristics that must be taken into account when performing memory transactions. In essence, Olarig is directed to a system for effectively eliminating the differences between two or more DIMMS, so that the remainder of

the system can treat all the memory modules as being uniform or identical. Thus, Olarig does not send different types of memory transactions to different memory modules, because his logic makes it unnecessary to distinguish between memory modules that have slightly different operating characteristics.

Olarig also fails to make any teachings at all regarding virtual memory. Virtual memory is a term of art. As disclosed in the specification at paragraph 0002, "Virtual memory is a commonly used technique that allows processes that are not stored entirely within main memory to execute by means of an automatic storage allocation scheme." The "Virtual Memory" article in Wikipedia, http://en.wikipedia.org/wiki/Virtual_memory, provides an excellent and efficient primer on this subject, and is recommended by the undersigned to the Examiner. It is noted that the pending claims do not read on computer systems that use conventional virtual memory because all memory transactions in those systems are directed to primary memory (sometimes called main memory). When data needed by a memory transaction is not currently present in primary memory, the virtual memory system "swaps" the data from secondary memory (typically disk storage) into primary memory, and then the memory transaction is performed using primary memory. The swapping of information between primary and secondary memory is performed "in the background." In the exemplary embodiment shown in Figure 1, the first and second memory devices 104 and 106 are both part of "main memory" – also called primary memory, as noted above.

Applicant's review of Olarig shows that the term 'virtual memory' is not even mentioned. While the Office Action cites column 25, lines 35-45 and column 26, lines 1-3 and 23-45 for claim limitations involving virtual memory, these portions of Olarig concern "address translation for multiple physical memory modules" within the main memory of the Olarig system. The multiple physical modules are coupled to the back end interface of the RAM personality module 300 and are the main memory of the Olarig system. Olarig's RAM "personality module 300 hides the actual physical structure at the back end 206 from the memory controller." Column 16, lines 44-45. There is no teaching in Olarig that the address translations performed by Olarig's personality module 300 are for virtual memory management, and in fact are used for completely distinct purposes.

Sinclair teaches a memory device having a user interface, a controller, a store, and an address mapping device. See, Abstract. In particular, Sinclair is concerned with repeatedly storing information in different locations in non-volatile memory while ensuring that

information can be recovered in the event of a power loss. Sinclair does not disclose anything relating to volatile memory much less first and second interfaces between each of first and second memory devices. Similarly, Sinclair does not disclose directing memory transactions to either a first or second memory interface depending on the characteristics of the transaction Like Olarig, Applicant's review of Sinclair shows that the term 'virtual memory' is not even mentioned. Thus Sinclair does not teach any of the limitations in the independent claims that Olarig fails to disclose.

Claims 1, 6-10, 13-14 And 31 Are Not Anticipated By Olarig

Claim 1 has been amended to recite a controller, comprising, *inter alia*, "a first memory interface adapted to be coupled to … volatile memory devices; a second memory interface adapted to be coupled to … non-volatile memory devices; and interface logic … configured … to direct memory transactions having … [one of a read-mostly characteristic and read-only characteristic] to the second memory interface." Claim 31 has been amended to recite a controller, comprising, *inter alia*, "a first interface means for coupling the controller to … volatile memory devices; a second interface means for coupling the controller to … non-volatile memory devices; and logic means … for directing memory transactions having … [one of a read-mostly characteristic and read-only characteristic] to the second memory interface."

Olarig does not disclose a controller having interfaces for both volatile and non-volatile memory devices and certainly does not disclose a memory controller having a second interface or interface means adapted to be coupled to one or more … non-volatile memory devices as claimed in amended claims 1 and 31. As discussed more fully above, the portion of Olarig cited in rejecting claim 2 describes prior art to Olarig and does not disclose a memory interface coupled to a second, non-volatile memory. Additionally, Olarig does not disclose interface logic configured to direct memory transactions having a read-mostly characteristic or read-only characteristic to the second memory interface, as claimed in claim 1. For at least these reasons, independent claim 1 and claims 6-10 and 13-14 which are dependent thereon and independent claim 31 are allowable over Olarig.

Claims 14-22, 24, 26-27 And 30-32 Are Not Anticipated By Olarig

Claims 14 and 15 recite, inter alia, "a processor having virtual memory logic for mapping virtual memory addresses into physical memory addresses and page logic for assigning physical memory addresses to virtual memory addresses, wherein the page logic is

configured to assign physical memory addresses in the one or more first memory devices to virtual memory addresses associated with a first usage characteristic, and to assign physical memory addresses in the one or more second memory devices to virtual memory addresses associated with a second usage characteristic." Claim 22 recites, inter alia, "establishing a plurality of page table entries, each entry in the plurality of page table entries mapping a virtual memory page address to a physical memory page address, each said entry including a usage field identifying a respective portion of main memory in which the physical memory page address is located, wherein the main memory includes at least two distinct portions." Claim 32 recites, inter alia, "virtual memory means for mapping virtual memory addresses into physical memory addresses and page means for assigning physical memory addresses to virtual memory addresses, wherein the page means assigned physical memory addresses in the one or more first memory devices to virtual memory addresses associated with a first usage characteristic, and assigns physical memory addresses in the one or more second memory devices to virtual memory addresses associated with a second usage characteristic." As discussed more fully above, Olarig does not disclose anything at all regarding virtual memory management, including virtual memory logic, virtual memory addresses, a virtual memory address, virtual memory means, or any of the claim limitations discussed above. For at least these reasons, claim 14, independent claim 15 and claims 16-21 which are dependent thereon, independent claim 22 and claims 24, 26-27 and 30 which are dependent thereon, and independent claim 32 are allowable over Olarig.

Olarig, Alone Or In Combination With Sinclair,
Does Not Teach All Of The Limitations Of Claims 1 And 2-32

As discussed above, Olarig fails to teach all of the limitations of the pending independent claims 1, 15, 22, 31 and 32. While the Office Action rejects dependent claims 3-5, 23 and 25 as being unpatentable over Olarig in view of Sinclair, as discussed above Sinclair also fails to teach all the limitations of the independent claims and so, in combination with Olarig, does not render any of the pending claims unpatentable. For at least these reasons, claims 3-5, 23 and 25 are patentable over Olarig in view of Sinclair.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 843-4000, if a telephone call could help resolve any remaining items.

Respectfully submitted,

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/ Gary S. Williams / 31,066

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